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Module ETH-LORA-M-AX-01
General Module Integration Guideline

For Ethertronics Module LORA-M-AX-01 (V1.2)

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OVERVIEW

This document provides hardware description about the Ethertronics LORA-M-AX-01 (V1.2) module. Simple applications for the module are detailed. These applications are using the Ethertronics Module associated with the Ethertronics Active Steering Antenna ETH-B2-01-ASA, in order to maximize the RF range.

The LORA-M-AX-01 (V1.2) can be used with three different interfaces:

- UART
- SPI[1]
- I2C[2]

Depending on the selected interface, the Ethertronics antenna control will need layout modifications.

[1]Coming soon with software update
[2]Coming soon with software update

GENERAL DESCRIPTION

PIN DIAGRAM

Note:

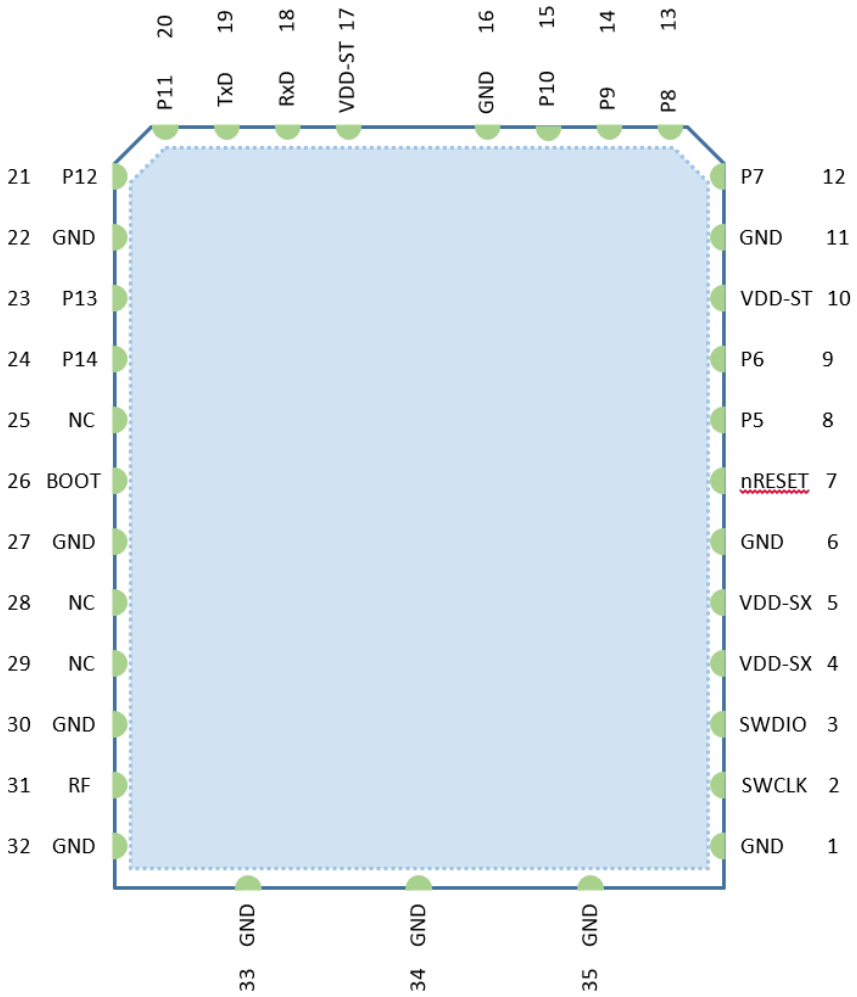

Figure 1

On the carrier board, the area under the Ethertronics module (light blue part on the Figure 1. PIN Diagram (Top View)) must be left without any conductive item (for example, gold plated vias) in order to avoid any short circuit.

PIN DESCRIPTION

Pin Number	Pin Name	Pin Type	MCU Pin	Description
1	GND	Supply		Ground Connection
2	SWCLK	Digital In/Out	PA14	Digital IO / JTCK / SWCLK
3	SWDIO	Digital In/Out	PA13	Digital IO / JTMS / SWDIO
4	VDD-SX	Supply		Supply Voltage for SX1272 part
5	VDD-SX	Supply		Supply Voltage for SX1272 part
6	GND	Supply		Ground Connection
7	nRESET	D In		nReset, internally pulled-up, internally filtered with capacitor
8	P5	Digital In/Out	PA11	Digital IO / USART1 CTS / MIPI DATA (See Table 2)
9	P6	Digital In/Out	PA12	Digital IO / USART1 RTS / MIPI CLK (See Table 2)
10	VDD-ST	Supply		Supply Voltage for ST part
11	GND	Supply		Ground Connection
12	P7	Digital In/Out	PB14	Digital IO / SPI2 MISO
13	P8	Digital In/Out	PB15	Digital IO / SPI2 MOSI / MIPI DATA (See Table 2)
14	P9	Digital In/Out	PB13	Digital IO / SPI2 CLK / MIPI CLK (See Table 2)
15	P10	Digital In/Out	PB12	Digital IO / SPI2 NSS / MIPI VIO (See Table 2)
16	GND	Supply		Ground Connection
17	VDD-ST	Supply		Supply Voltage for ST part
18	RxD	Digital In/Out	PA10	Digital IO / USART1 RX
19	TxD	Digital In/Out	PA9	Digital IO / USART1 TX / MIPI VIO (See Table 2)
20	P11	Digital In/Out	PA3	Stop Mode Wake Up / Digital IO
21	P12	Digital In/Out	PB8	Digital IO / I2C1-SCL / Interface Selection (See Table 2)
22	GND	Supply		Ground Connection
23	P13	Digital In/Out	PB9	Digital IO / I2C1-SDA / Interface Selection (See Table 2)
24	P14	Digital In/Out	PC13	Digital IO / AS VDD
25	NC	NC		
26	BOOT	D In	BOOT0	Bootloader Pin 0, internally pulled down
27	GND	Supply		Ground Connection
28	NC	NC		
29	NC	NC		
30	GND	Supply		Ground Connection
31	RF	RF In/Out		LoRa Antenna Port
32,33,34,35	GND	Supply		Ground Connection

Table 1

INTERFACE SELECTION

P12 State	P13 State	Selected Interface	PIN Name	Pin Function
Pulled-Up	Pulled-Up	I2C MIPI uses SPI Pins	P5	USART1-CTS
			P6	USART1-RTS
			P8	MIPI DATA
			P9	MIPI CLK
			P10	MIPI VIO
			TxD	USART1-TX
			P12	Interface Selection / I2C1-SCL
			P13	Interface Selection / I2C1-SDA
Pulled-Up	Pulled-Down	Reserved		
Pulled-Down	Pulled-Up	UART MIPI uses SPI Pins	P5	USART1-CST
			P6	USART1-RTS
			P8	MIPI DATA
			P9	MIPI CLK
			P10	MIPI VIO
			TxD	USART1-TX
			P12	Interface Selection
			P13	Interface Selection
Pulled-Down	Pulled-Down	SPI MIPI uses UART Pins	P5	MIPI DATA
			P6	MIPI CLK
			P8	SPI2 MOSI
			P9	SPI2 CLK
			P10	SPI2 NSS
			TxD	MIPI VIO
			P12	Interface Selection
			P13	Interface Selection

Table 2

RECOMMENDED LANDING PATTERN

Below is the recommended landing pattern. The Ethertronics customer Eagle Library, containing the LORA-M-AX-01 (V1.2) part, can be found on Ethertronics webpage. Always remember to leave the top layer of the board without any conductive element (signal vias, pad …) below the module to avoid short circuit with the module ground.

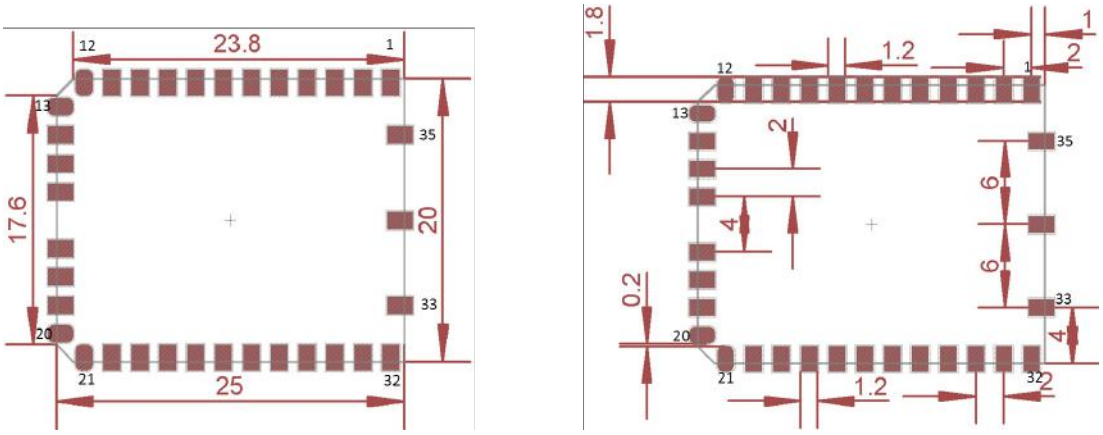

Figure 2

TYPICAL APPLICATION SCHEMATICS

As the LORA-M-AX-01 V1.2 module can be set using three interfaces (UART, SPI and I2C), three typical application schematics are presented.

The LORA-M-AX-01 V1.2 has been designed to be easy to implement on a PCB.

- All decoupling capacitors are already mounted on the module,
- all pull-up or pull-down resistors are also mounted and filtering capacitors too.
- The most critical thing is to double check that the supply voltage used is meeting the datasheet specifications.

UART INTERFACE APPLICATION

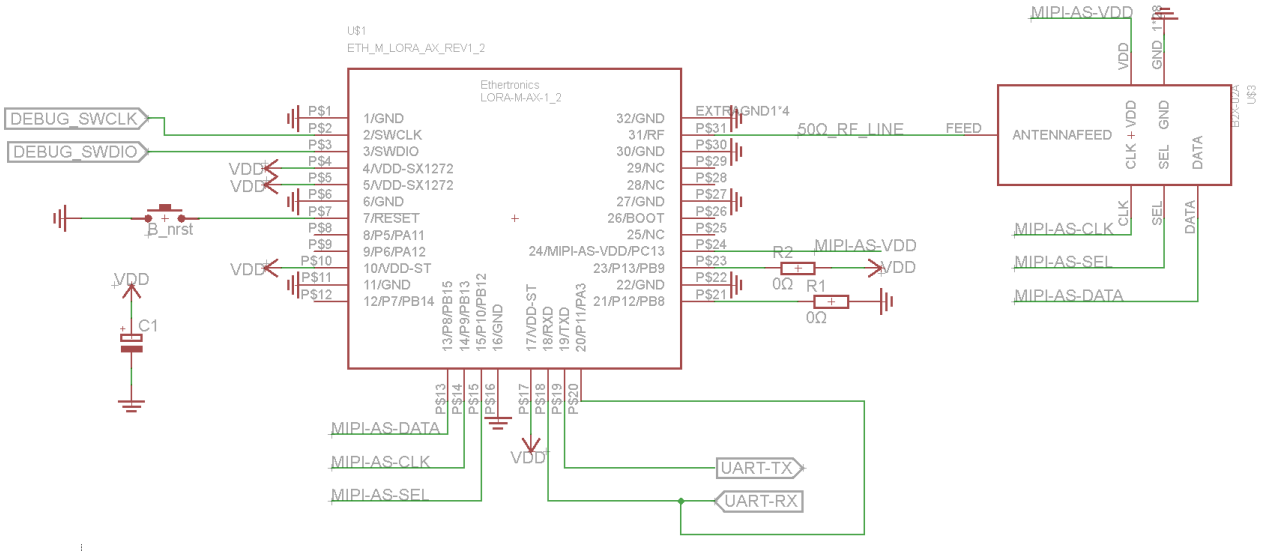

Figure 3

UART INTERFACE APPLICATION BOM

Schematic Part Name	Manufacturer	Manufacturer Part Number	Description
U$1	Ethertronics, Inc.	LORA-M-AX-01	Lora Module V1.2
U$3	Ethertronics, Inc.	B2	Active Steering Antenna (MIPI Interface)
B_nrst	Rafi	1.14002.1010000	SWITCH PUSH SPST-NO 0.1A 35V
R1	Panasonic	ERJ-S020R00X	Thick Film Resistors - SMD 0402 Zero ohm Jumper 0.05ohm AEC-Q200
R2	Panasonic	ERJ-S020R00X	Thick Film Resistors - SMD 0402 Zero ohm Jumper 0.05ohm AEC-Q200
C1	Nichicon	UUX1C101MNL1GS	Aluminium Electrolytic Capacitors - SMD 16volts 100uF Snap-In Audio

Table 3

UART-RX signal is also connected to P11 in order to wake up the module when using the stop mode for low power mode.

SPI INTERFACE APPLICATION

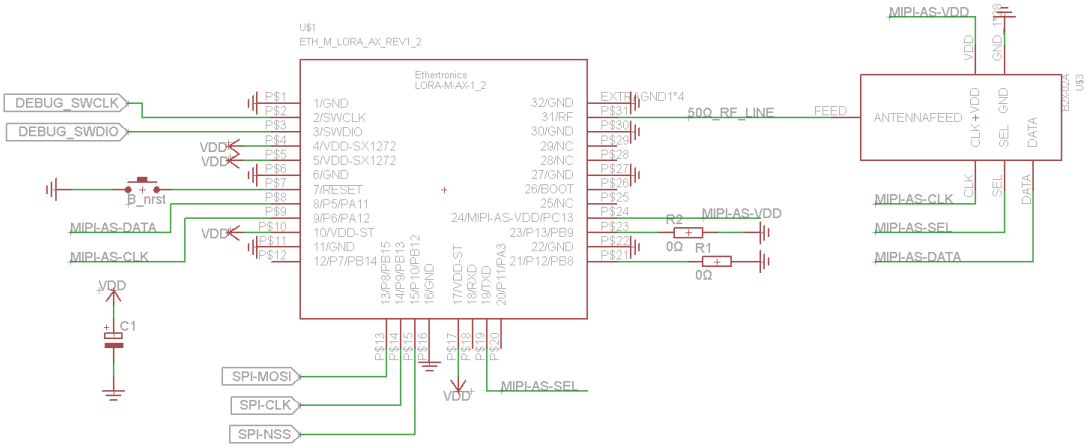

Figure 4

SPI INTERFACE APPLICATION BOM

Schematic Part Name	Manufacturer	Manufacturer Part Number	Description
U$1	Ethertronics, Inc.	LORA-M-AX-1_2	Lora Module V1.2
U$3	Ethertronics, Inc.	B2	Active Steering Antenna (MIPI Interface)
B_nrst	Rafi	1.14002.1010000	SWITCH PUSH SPST-NO 0.1A 35V
R1	Panasonic	ERJ-S020R00X	Thick Film Resistors - SMD 0402 Zero ohm Jumper 0.05ohm AEC-Q200
R2	Panasonic	ERJ-S020R00X	Thick Film Resistors - SMD 0402 Zero ohm Jumper 0.05ohm AEC-Q200
C1	Nichicon	UUX1C101MNL1GS	Aluminium Electrolytic Capacitors - SMD 16volts 100uF Snap-In Audio

Table 4

I2C INTERFACE APPLICATION

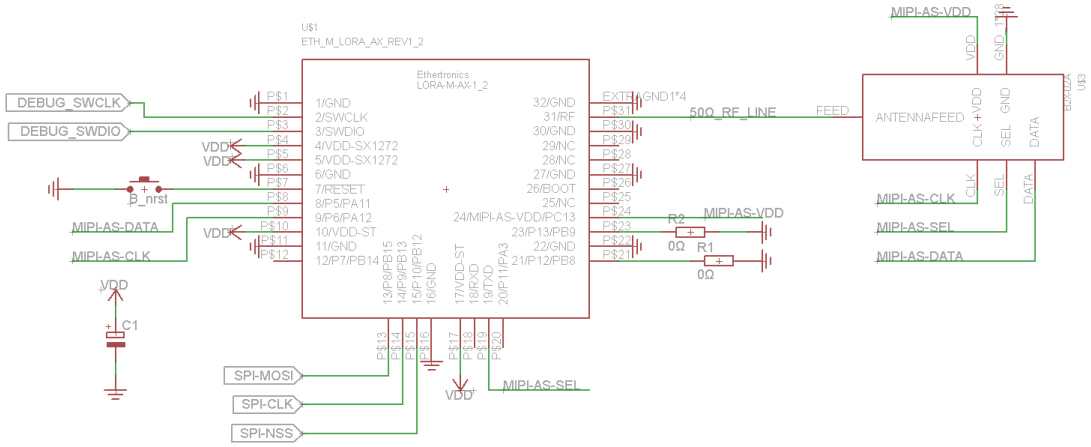

Figure 5

I2C INTERFACE APPLICATION BOM

Schematic Part Name	Manufacturer	Manufacturer Part Number	Description
U$1	Ethertronics, Inc.	LORA-M-AX-01	Lora Module V1.2
U$3	Ethertronics, Inc.	B2	Active Steering Antenna (MIPI Interface)
B_nrst	Rafi	1.14002.1010000	SWITCH PUSH SPST-NO 0.1A 35V
R1	Panasonic	ERJ-S020R00X	Thick Film Resistors - SMD 0402 Zero ohm Jumper 0.05ohm AEC-Q200
R2	Panasonic	ERJ-S020R00X	Thick Film Resistors - SMD 0402 Zero ohm Jumper 0.05ohm AEC-Q200
C1	Nichicon	UUX1C101MNL1GS	Aluminium Electrolytic Capacitors - SMD 16volts 100uF Snap-In Audio

Table 5

PCB DESIGN AND GENERAL USE GUIDE LINE

RF DESIGN GUIDE LINE

The RF pin of the LORA-M-AX-01 V1.2 is matched to 50Ω by default. The used antenna should also be matched to 50 Ω.

Even if the LORA-M-AX-01 embeds an impedance tuner to correct and minimize impedance detuning when the environment of the module changes, it is better to have the antenna match to 50 Ohms in its original configuration.

Eventually, additional matching components can to be added between the RF pin of the LORA-M-AX-01 module and the antenna feed.

To have an ideal transmission between the module and the antenna, the line should be as short as possible and has an impedance of 50Ω. Avoid any sharp angle on this line, by having at maximum 45° angles. The impedance of the line can be calculated, depending on the frequency and the PCB material and dimensions. For a grounded coplanar line (recommended line structure), the impedance depends on:

- The frequency
- The clearance between the line and the same layer ground (S)
- The line width (**W**)
- The metallization thickness (**T**)
- The height of the substrate or distance between top layer and underneath ground (H)
- The substrate permittivity (**εr**)
- The substrate loss tangent (**tan δ**)

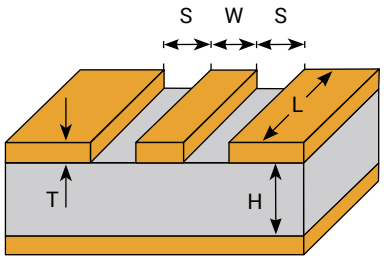

Figure 6

The ground on the top layer and the ground on the layer below the RF line must be connected with as many vias as possible.

If all the above recommendations are not followed for any reason, be advised that the RF performances, such as sensitivity, range, output power, could be deteriorated.

SUPPLY GUIDE LINE

All the GND pins of the LORA-M-AX-01 (V1.2) module have to be connected to the main board ground in order to reduce the risk of unwanted external noise on the module. In the same way, all the VDD pins have to be connected to the power supply in order to have minimum voltage variation during Transmit burst.

The LORA-M-AX-01 contains several vias, and these vias are not covered by solder resist on the bottom layer. Therefore, to avoid any short circuit, be advised that the top layer of the PCB board should be totally free of any exposed pads or gold plated vias.

The ETH-LORA-M-AX-01 (V1.2) electrical parameters are listed in the table below. All decoupling capacitors are already mounted on the module. However, for specific reasons and uses, it can be useful to add more decoupling element. It is therefore useful to add capacitor pads between the VDD pins of the ETH-LORA-

	Min.	Typ.	Max.	Unit
Supply Voltage (VDD)	2.5	3.0	3.6	V
Current Consumption Stop mode with RTC	-	1.8	-	mA
Current Consumption Sleep Mode	-	3	-	mA
Current Consumption Run Mode	-	9	-	mA
Current Consumption TX Mode	-	100	-	mA
Current Consumption RX Mode	-	20	-	mA

Table 6

M-AX-01 (V1.2) and the ground of the main board, even if components are not mounted later.

In order to have the most stable supply as possible, it is highly recommended to use a Low Drop Out (LDO) between the power supply and the VDD of the PCB. The maximum consumption of the ETH-LORA-M-AX-01 (V1.2) is 128mA during transmission. However, high current peak can appear during LoRa RF burst, and it is advised to use a LDO delivering up to 2A in order to insure the good running of the module.

UART GUIDE LINE

Parameter	Baud Rate	Data Length	Parity	Stop Bit	Flow Control
Default Value	115200	8 bits	None	1 bit	None

Table 7

The ETH-LORA-M-AX-01 (V1.2) UART has a default 115200 Baud rate. In order to maximize the UART performances, Tx and Rx lines must be routed in parallel with a constant distance. They also need to be routed symmetrically. Try to minimize the area in which the specified spacing is enlarged du to pads entries. Avoid placing any components between the lines, even if the signals are routed symmetrically.

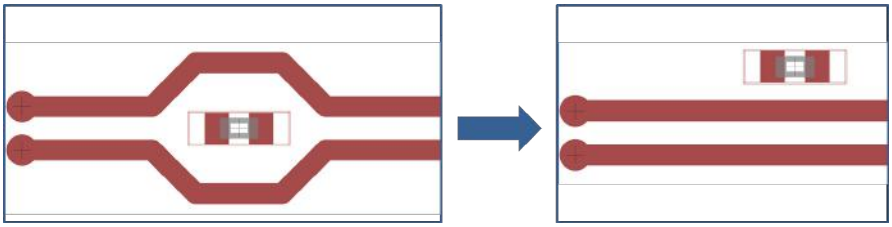

Figure 7

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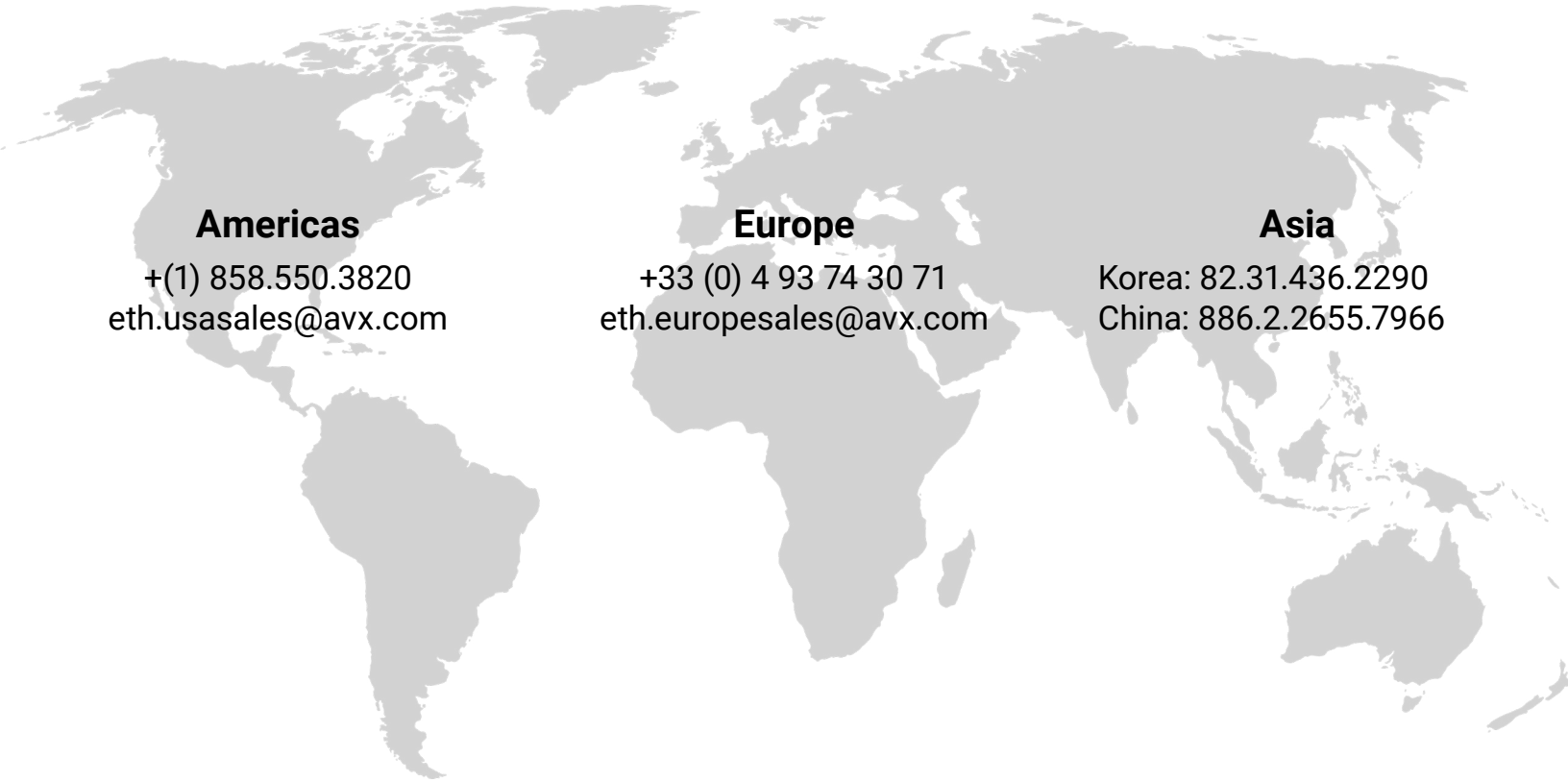

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